Amendments to the Claims

This listing of the claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended): A level-shifting circuit, comprising:

a level modulating circuit having an input terminal and an inverse input terminal for respectively receiving a complementary pair of small signals, and a first output terminal for outputting a voltage level in response to the complementary pair of small signals, wherein the level modulating circuit comprises:

a first PMOS transistor having a first gate coupled to the input terminal, a first source coupled to a power source and a first drain as the second output terminal;

a second PMOS transistor having a second gate coupled to the inverse input terminal, a second source coupled to the power source and a second drain as the first output terminal;

a first NMOS transistor having a third gate coupled to the power source, a third drain coupled to the first drain and a third source as the inverse input terminal; and

a second NMOS transistor having a fourth gate coupled to the power source, a fourth drain coupled to the second drain and a fourth source as the input terminal; and

an enable circuit ~~coupled to the first output terminal and~~ making the first output terminal output a predetermined voltage level signal when receiving a disable signal, wherein the enable circuit comprises:

a MOS transistor having a fifth source and a fifth drain coupled between an external level and one of the first output terminal and the second output terminal, and a fifth gate coupled to the disable signal; and

a pair of third NMOS transistors having six drains respectively coupled to the input terminal and the inverse input terminal, six sources coupled to the complementary pair of small signals, and six gates coupled to the disable signal.

2. (Canceled)

3. (Currently Amended): The level-shifting circuit as claimed in claim 1, wherein the MOS transistor ~~enable circuit~~ is a ~~first~~ third PMOS transistor having the fifth source coupled to [[a]]the power source, and the fifth drain coupled to the first output terminal.

4. (Currently Amended): The level-shifting circuit as claimed in claim 1, wherein the MOS transistor ~~enable circuit~~ is a ~~first~~ fourth NMOS transistor having the fifth source coupled to a ground level, and the fifth drain coupled to one of the first output terminal and the [[a]] second output terminal.

5-6. (Canceled)

7. (Currently Amended): The level-shifting circuit as claimed in claim [[6]]3, wherein the enable circuit further comprises an inverter coupled between the gates of the ~~first and~~ third and fourth NMOS transistors.

8. (Canceled)

9. (Currently Amended): A level-shifting circuit, comprising:

a level modulating circuit having a first input terminal for receiving a reference signal and a second input terminal for receiving a modulating signal, and an output terminal for outputting a voltage level in response to the level of the modulating signal, wherein the level modulating circuit comprises:

a first PMOS transistor having a first gate coupled to the input terminal, a first source coupled to a power source and a first drain as the second output terminal;

a second PMOS transistor having a second gate coupled to the inverse input terminal, a second source coupled to the power source and a second drain as the first output terminal;

a first NMOS transistor having a third gate coupled to the power source, a third drain coupled to the first drain and a third source as the inverse input terminal; and

a second NMOS transistor having a fourth gate coupled to the power source, a fourth drain coupled to the second drain and a fourth source as the input terminal; and

an enable circuit ~~coupled to the output terminal and~~ making the output terminal output a predetermined voltage level signal when receiving a disable signal, wherein the enable circuit comprises:

a thin film transistor (TFT) having a fifth source and a fifth drain coupled between an external level and the output terminal, and a fifth gate coupled to the disable signal; and

a pair of first N-type thin film transistors having sixth drains respectively coupled to the first and second input terminals, sixth sources respectively receiving the reference signal and the modulating signal, and sixth gates coupled to the disable signal.

10. (Canceled)

11. (Currently Amended): The level-shifting circuit as claimed in claim 9, wherein the thin film transistor ~~enable circuit~~ is a first P-type thin film transistor having the fifth source coupled to a power source, and the fifth drain coupled to the first output terminal.

12. (Currently Amended): The level-shifting circuit as claimed in claim 9, wherein the thin film transistor ~~enable circuit~~ is a ~~first~~ second N-type thin film transistor having the fifth source coupled to a ground level, and the fifth drain coupled to [[a]]the ~~second~~ first output terminal.

13-14. (Canceled)

15. (Currently Amended): The level-shifting circuit as claimed in claim [[9]]12, wherein the enable circuit further comprises an inverter coupled between the gates of the first N-type thin film transistors and the ~~third~~ second N-type thin film NMOS transistor.

16. (Previously presented): The level-shifting circuit as claimed in claim 1, wherein said predetermined voltage level signal is fixed.

17. (Previously presented): The level-shifting circuit as claimed in claim 9, wherein said predetermined voltage level signal is fixed.

18. (Currently amended): A level-shifting circuit, comprising:

a level modulating circuit having an input terminal and an inverse input terminal for respectively receiving a complementary pair of signals, and a first output terminal for outputting a first voltage level in response to the complementary pair of signals, wherein the level modulating circuit comprises:

a first PMOS transistor having a first gate coupled to the input terminal, a first source coupled to a power source and a first drain as the second output terminal;

a second PMOS transistor having a second gate coupled to the inverse input terminal, a second source coupled to the power source and a second drain as the first output terminal;

a first NMOS transistor having a third gate coupled to the power source, a third drain coupled to the first drain and a third source as the inverse input terminal; and

a second NMOS transistor having a fourth gate coupled to the power source, a fourth drain coupled to the second drain and a fourth source as the input terminal; and

an enable circuit ~~coupled to the first output terminal to cause~~ causing the first output terminal to output a second voltage level signal independent of the first voltage level, wherein the enable circuit comprises:

a MOS transistor having a fifth source and a fifth drain coupled between an external level and the first output terminal, and a fifth gate coupled to a disable signal; and

a pair of third NMOS transistors having six drains respectively coupled to the input terminal and the inverse input terminal, six sources coupled to the complementary pair of signals, and six gates coupled to the disable signal.

19. (Canceled)

20. (Currently amended): The level-shifting circuit as claimed in claim 18, wherein the MOS transistor ~~enable circuit~~ is a third PMOS transistor having the fifth source coupled to [[a]]the power source, and the fifth drain coupled to the first output terminal.